$\varphi_2(s)$ and, if appropriate, for the amplitudes $E_1(s)$ and $E_2(s)$.

It is an object of the invention to create a device with the aid of which FSM bits can be determined as a function of the mode and slot index in a particularly efficient fashion. A corresponding method for calculating the FSM bits is also to be specified.

The objects on which the invention is based are achieved by means of the features of the independent patent claims 1 and 15. Advantageous developments and refinements of the invention are specified in the subclaims.

The device according to the invention serves for calculating FSM bits by means of which the signals sent from two antennas of a base station are influenced with reference to their phase difference and/or their amplitudes. The FSM bits are calculated with the aid of two estimated channel impulse responses. In this process, a channel impulse response is related in each case to the channel belonging to one of the antennas. An essential idea of the invention resides in the fact that the device is hard-wired. It is therefore present as a hardware circuit.

Owing to the hardware design of the device according to the invention, the latter can carry out the required calculations substantially more efficiently than a digital signal processor. Furthermore, the device according to the invention is more favorable in terms of outlay than a digital signal processor.

The device preferably forms a complex phasor from components of the two channel impulse responses and then generates an FSM bit by means of rotation and projection of the phasor and, in particular, of a threshold value decision. In particular, the channel coefficients, which are combined in a channel impulse response for each channel, can

Patent Claims

1. A device (1) for calculating FSM bits (FSM(s)) by means of which the signals sent from two antennas of a base station are influenced with reference to their phase difference and/or their amplitudes with the aid of two estimated channel impulse responses ($h_{1,n}(s)$, $h_{2,n}(s)$), the device (1) being present in hard-wired form.

2. The device (1) as claimed in claim 1, characterized
- in that a complex phasor (H_{21}) is formed from components ($h_{1,n}(s)$, $h_{2,n}(s)$) of the two channel impulse responses, and
- in that an FSM bit (FSM(s)) is produced by means of rotation and projection of the phasor (H_{21}) and, in particular, of a threshold value value decision.

3. The device (1) as claimed in claim 1 or 2, characterized
- in that components ($h_{1,n}(s)$, $h_{2,n}(s)$) of the two channel impulse responses can be applied at inputs (In1, ..., In4) of the device (1),
- in that control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$) can be applied at control inputs (Config1, ..., Config6) of the device (1), and
- in that the FSM bit (FSM(s)) can be tapped at an output of the device (1), the FSM bit (FSM(s)) being calculated as a function of the components ($h_{1,n}(s)$, $h_{2,n}(s)$) of the two channel impulse responses and the control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$).

4. The device (1) as claimed in claim 3, characterized
- by a logic unit (2, 3) and a processing unit (4, ..., 9) connected downstream of the logic unit (2, 3).

5. The device (1) as claimed in claim 4, characterized
- in that components ($h_{1,n}(s)$, $h_{2,n}(s)$) of the two channel impulse responses are present at inputs (In1, In2, In3, In4) of the logic unit (2, 3),
- in that the logic unit (2, 3) has outputs (Out1, Out2, Out5, Out6) whose number is equal to the number of its inputs (In1, In2, In3, In4), and
- in that the inputs (In1, In2, In3, In4) of the logic unit (2, 3) can be connected to the outputs (Out1, Out2, Out5, Out6) of the logic unit (2, 3) as a function of at least one of the control signals ($C_{1,k}(s)$, ..., $C_{5,k}(s)$).

6. The device (1) as claimed in claim 4 or 5, characterized
- in that a multiplier stage (4, 5), an adder (6), a weighting stage (7), an accumulator (8) and a threshold value value decision unit (9) are connected in series in the prescribed sequence in the processing unit (4, ..., 9).

7. The device (1) as claimed in claim 6, characterized
- in that the multiplier stage has two multipliers (4, 5) whose inputs are connected in each case to two outputs (Out1, Out2, Out5, Out6) of the logic unit (2, 3), and
- in that the inputs of the adder (6) are connected to the outputs of the multipliers (4, 5).

8. The device (1) as claimed in claims 6 and 7, characterized
- in that a control signal ($C_{6,k}(s)$) is present at the weighting stage (7), and
- in that the weighting stage (7) applies a weighting factor to the sum (S_k) formed by

the adder (6), doing so as a function of the control signal ($C_{6,k}(s)$) present at it.

9. The device (1) as claimed in one or more of claims 3 to 8, characterized
- in that the control signals are stored in the form of control bits ($C_{1,k}(s)$, ..., $C_{6,k}(s)$) in a read-only memory.

10. The device (1) as claimed in one or more of the preceding claims, characterized
- in that the device (1) is designed for the UMTS standard.

11. The device (1) as claimed in claim 10, characterized
- in that the control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$) are a function of the slot number (s) of the FSM bit (FSM(s)) to be calculated, and of the CLTD mode.

12. The device (1) as claimed in claim 10 or 11, characterized
- in that the control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$) are a function of whether the slot number (s) of the FSM bit (FSM(s)) to be calculated is an even or odd number.

13. A mobile radio terminal having a device (1) as claimed in one or more of the preceding claims.

14. A method for calculating FSM bits (FSM(s)) by means of which the signals sent from two antennas of a base station are influenced with reference to their phase difference and/or their amplitudes with the aid of two estimated channel impulse responses ($h_{1,n}(s)$, $h_{2,n}(s)$), having the following steps:
(a) producing a complex phasor (H_{21}) from components ($h_{1,n}(s)$, $h_{2,n}(s)$) of the two channel impulse responses; and

(b) calculating an FSM bit (FSM(s)) by rotation and projection of the phasor (H_{21}).

15. The method as claimed in claim 14, characterized
- in that the rotation and projection of the phasor (H_{21}) is determined by control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$).

16. The method as claimed in claim 14 or 15, characterized
- in that a threshold value value decision is carried out after the rotation and projection of the phasor (H_{21}) in order to calculate the FSM bit (FSM(s)).

17. The method as claimed in one or more of claims 14 to 16, characterized
- in that the method is designed for the UMTS standard.

18. The method as claimed in claims 15 and 17, characterized
- in that the control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$) are a function of the slot number (s) of the FSM bit (FSM(s)) to be calculated, and of the CLTD mode.

19. A method as claimed in claim 18, characterized
- in that the control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$) are a function of whether the slot number (s) of the FSM bit (FSM(s)) to be calculated is an even or odd number.

Abstract

Device for calculating FSM bits in the UMTS standard

The invention relates to a device (1) for calculating FSM bits (FSM(s)) by means of which the signals sent from two antennas of a base station are influenced with reference to their phase difference and/or their amplitudes. The FSM bits (FSM(s)) are calculated with the aid of two estimated channel impulse responses ($(h_{1,n}(s), h_{2,n}(s))$. The device (1) is present in hard-wired form.

(Figure 1 for the abstract)